A novel technique to minimize stand by leakage power in nanoscale CMOS VLSI

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ABSTRACT

This paper proposes a novel approach to minimize leakage currents in CMOS circuits during the off-state (or standby mode, sleep mode) by applying the optimal reverse body bias to the substrate (body or bulk) to increase the threshold voltage of transistors. The optimal bias point is determined by comparing the sub-threshold current ($I_{SUB}$) and band-to-band current ($I_{BTBT}$) simultaneously. The proposed circuit was simulated in HSPICE using 90nm bulk CMOS technology and evaluated using ISCAS85 benchmark circuits at different operating temperature (ranging from 25°C to 100°C). Analysis of the results shows a maximum of 551 and 1491 times leakage power reduction at 25°C and 100°C on a circuit with 546 gates. The proposed approach demonstrates that the optimal body bias reduces considerable amount of the leakage power in the nanoscale CMOS integrated circuits. In this approach, the temperature and supply voltage variations are compensated by the proposed feedback loop.

Keywords: off-state, standby mode, sleep mode, leakage currents, sub-threshold leakage current, band-to-band tunneling (BTBT) leakage current.

Key words: Leakage power, Nanoscale CMOS technology.

INTRODUCTION

Over the past four decades there has been the continuous reduction in the size of the transistors to increase the speed and density of the devices on a given chip and the die yield during manufacturing. To sustain device reliability and minimize power consumption, the supply voltage has been reduced as well. Accordingly, the threshold voltages of the transistors had to be scaled down to maintain the high drive current and hence performance improvements. However, the threshold voltage reduction has caused substantial increase in subthreshold leakage current, which severely affects the standby power dissipation. To suppress the subthreshold leakage current ($I_{SUB}$), reverse body biasing (RBB) technique has been widely employed to increase the threshold voltage ($V_{th}$) during the offstate. However, this technique also increases the short channel effects ($SCE_{s}$) such as Drain induced barrier lowering (DIBL), Gate-induced drain leakage ($IGIDL$) and band-to-band tunneling ($I_{BTBT}$) current. Since the state-of-the-art MOSFETs are fabricated with the increased overall doping concentration, lowered source/drain junction depths, halo doping, high-mobility channel materials and etc., these techniques increase both $IGIDL$ and $I_{BTBT}$ significantly under the reverse body bias condition. Furthermore, the reduction of the gate oxide thickness causes drastic increase in the gate tunneling leakage current ($I_{G}$) due to carrier tunneling through the gate oxide, which is a strong exponential function of the voltage magnitude across the gate oxide. Therefore, in order to minimize the leakage power in standby mode, all leakage components ($I_{SUB}$, $I_{BTBT}$ and $I_{G}$) should be taken into account in RBB technique. This paper proposes a new circuit to determine the optimal
reverse body bias so as to minimize the off-state leakage power consumption by comparing extracted sub-threshold leakage current \( (I_{\text{SUB}}) \) component with band-to-band tunneling leakage current \( (I_{\text{BTBT}}) \) component simultaneously. In the proposed circuit, the \( I_{\text{SUB}}, I_{\text{G}}, I_{\text{GIDL}}, \) and \( I_{\text{BTBT}} \) leakage currents are fully monitored and controlled under the process, voltage, and temperature (PVT) variations. The experimental results show a considerable energy reduction in nanoscale CMOS circuits.

**Leakage current components in nMOSFET at off-state**

Total leakage current \( (I_T) \) in the off-state nMOSFET is represented as

\[
I_T = I_{\text{SUB}} + I_{\text{BTBT(DB)}} + I_{\text{BTBT(SB)}} + I_{\text{GIDL(DB)}} + I_{\text{GIDL(SB)}} + I_{\text{GB-IDG}}
\]

... (1)

where, \( I_{\text{SUB}} \) is Sub-threshold leakage current, \( I_{\text{BTBT(DB)}} \) and \( I_{\text{BTBT(SB)}} \) are band-to-band tunneling leakage currents (drain-to-bulk and source-to-bulk reverse-bias pn junction leakage currents), \( I_{\text{GIDL(DB)}} \) and \( I_{\text{GIDL(SB)}} \) are Gate-Induced Drain Leakage current, \( I_{\text{GB}} \) is gate-to-bulk oxide tunneling leakage current, and \( I_{\text{IDG}} \) is drain-to-gate oxide tunneling leakage current.

The variation of the total gate leakage current \( (I_G = I_{\text{GB}} - I_{\text{IDG}}) \) is negligible for the reverse bias voltage ranging from 0V to -2V as shown in Figure 2. This means that the variation of \( I_{\text{GB}} \) is insignificant since \( I_{\text{IDG}} \) is independent of the reverse-body bias. For convenience, let’s denote that \( I_{\text{BTBT1}} = I_{\text{GIDL(DB)}} + I_{\text{BTBT(DB)}} \), \( I_{\text{BTBT2}} = I_{\text{GIDL(SB)}} + I_{\text{BTBT(SB)}} \), and \( I_{\text{BTBT}} = I_{\text{BTBT1}} + I_{\text{BTBT2}} \). Figure 2 below shows leakage currents of the 32nm n-MOSFET transistor when \( V_{GS} = 0 \)V as a function of body bias voltage and supply voltage.

**The dependencies of leakage currents on reverse-body biasing**

A device is in the off-state when it is operating well below the threshold \( (V_{T} \approx 0) \). However, even in the off-state, some small current flow occurs and this off-state current can result in considerable power dissipation in an integrated circuit with millions of transistors. Therefore, taking into consideration the value of the sub-threshold leakage current is very important. The weak inversion sub-threshold current can be expressed based on the Equation (2) [6].

\[
V_{th} = V_{th(0)} + V_T (1 - \phi - F + \phi(SB)) - \sqrt{1 - 2\phi - F} \]

... (4)

Where the body-effect coefficient, \( q \) is the electron charge, \( s i \) is the permittivity of Si, \( N_{SUB} \) is the doping concentration of the substrate, \( \phi(F) \) is the Fermi potential and equal to \( (kT/q) \ln\left(\frac{N_{SUB}}{n_i}\right) \), and \( V_{SB} \) is the source to bulk potential difference.

As shown in Equation (2), sub-threshold leakage current increases exponentially as \( V_{th} \) reduces. To suppress the subthreshold leakage current \( (I_{\text{SUB}}) \), reverse body biasing (RBB) technique can be used to increase the threshold voltage \( (V_{th}) \) in standby mode CMOS circuits. \( V_{SB} \) becomes more positive by increasing the reverse body bias, which results in higher threshold voltage and exponential decrease of the subthreshold current as explained in Equation (2) and (4). Figure 2 explains why the leakage power consumption of the chip does not continue to reduce monotonically as the value of reverse bias increases. Figure 3 shows the effect of body bias voltage and supply voltage on leakage power for a CMOS transistor of 32nm CMOS technology. At around -0.9 to -2.2 body bias voltage, the leakage power increases due to highly increased \( I_{\text{BTBT}} \). \( I_{\text{G}} \) has less effect on the power variation. As a result, there is an optimal reverse body bias point which makes a minimal total standby leakage power of a device for each different supply.
voltage. This optimal point occurs when the sum of both the sub-threshold and band-to-band-tunneling currents has the minimum value as shown in Fig. 2 and 3.

Sub-threshold leakage current suppression using stack effect

Sub-threshold leakage current is reduced when there are two or more stacked off-transistors. By turning off more than one transistor in a stack of transistors, it forces the intermediate node voltage to have a value higher than zero. This causes a negative $V_{gst}$, $V_{gs}$ (more body effect) and $V_{ds}$ reduction (less DIBL) in the top transistor, thereby helping reduce the sub threshold leakage current flowing through the stack considerably, which is known as the stack effect and this results in reduced sub-threshold leakage current. Figure 4 and Figure 5 illustrate the leakage current trends of each stacked transistors as a function of the stacked transistor number [8], [9].

Optimal body monitoring circuit

Reverse body biasing (RBB) has widely been used to reduce the leakage power of devices. However, most recent research has shown that if RBB is too high, leakage power can actually increase due to the contribution of the band-to-band tunneling currents. To prevent this problem a new optimal body biasing system is required to balance the sub-threshold leakage with the BTBT leakage. The proposed system increases $V_{th}$ by adjusting body voltage in the RBB direction so as to reduce sub-threshold leakage current. When the optimum body bias is detected, the body voltage adjustments are stopped to avoid excessive reverse body bias. Figure 6 shows the proposed method to reduce the leakage current of the nanometer CMOS circuits. The system consists of three stages; 1) Leakage Monitoring Circuit, 2) Current Comparator, and 3) Charge Pump [7].

The leakage monitoring circuit separates the subthreshold leakage (ISUB) and BTBT leakage current (IBTBT1, 2) from the total leakage components. Fig. 7 shows a new leakage monitoring circuit with NMOS transistors, where the transistors, MN2, MN7, and MN12 are the replica circuits to generate leakage components, and MP0/MP1, MP2/MP3, and MN10/MN11 form current mirrors. By using triple off-transistors in a stack, we can ignore the subthreshold current flowing from drain to source of MN2 transistor. Thus the amount of drain current of MN2 transistor notated as $I_2$ is approximately the same as the sum of $I_{DG}$ and $I_{BTBT1}$. The drain current of MN7 notated as $I_1$ consists of $I_{DG}$, $I_{BTBT1}$, and $I_{SUB}$. In the source of the MN12 transistor, the current $I_3$ consisting of

<table>
<thead>
<tr>
<th>Circuit</th>
<th># of gates</th>
<th>Function</th>
<th>Leakage (µW): Temperature = 25°C</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Zero body Bias</td>
</tr>
<tr>
<td>C432</td>
<td>160</td>
<td>27-channel interrupt controller</td>
<td>5.880</td>
</tr>
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<td>202</td>
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<td>88-</td>
<td>16-bit SEC/DED circuit</td>
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<td>546</td>
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<td>49.687</td>
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Table 1: Experimental results for leakage power
Fig. 1: Leakage current components in the Off-state under reverse body bias

Fig. 2 Leakage currents of 90nm nMOSFET with 0.9nm oxide thickness and (W/L) = (128nm/32nm). (a) IG (b) ISUB, IBTBT, and IBTBT + ISUB (c) Total Leakage current = ISUB + IBTBT + IG
Fig. 3: Leakage Power of NMOS Device under Reverse Body

Fig. 4: Leakage current descendant with the increasing number of off transistors in stack (where, VDD = 0.9V is applied to 32nm nMOSFETs with 0.9nm oxide thickness and (W/L) = (128nm/32nm))

Fig. 5: Sub-threshold leakage current difference among (a) a single off transistor, (b) a stack of two off-transistors, and (c) a stack of two off-transistors with reverse-body bias. The barrier height increases for the two-stack transistors (b) and further increases for the two-stack transistor (b) and future increases for the two-stack off-transistor with reverse body bias (c) due to a smaller VDS (Vm<VDD) and the applied reverse-body bias.
IDG, IBTBT2, and ISUB is generated. The leakage monitoring circuit for PMOS device is made up of the same structure as the monitoring circuit for NMOS device.

Two current differential amplifiers are employed based on the generated leakage components. $I_{\text{sub}}$ (current $I_1$–current $I_2$) is obtained through MN4, MN5, and MN6 transistors while $I_{\text{BTBT}} = I_{\text{BTBT1}} + I_{\text{BTBT2}}$ (current $I_1$–current $I_3$) is obtained through MN8, MN9, and MN10 transistors. The separated leakage components are applied to the current comparator to generate pulse width proportional to the magnitude of each leakage. Then, depending on the two signals from the current comparator and its own bias voltage, the charge pump discharges or charges its output capacitor. The current comparator-based circuit provides the optimal body-bias voltage to match $I_{\text{sub}}$ with $I_{\text{BTBT}}$ ($=I_{\text{BTBT1}} + I_{\text{BTBT2}}$).

**RESULTS**

The proposed method was simulated in HSPICE using 32nm technology and evaluated using ISCAS85 benchmark circuits
for different operating temperature range from 250°C to 1000°C. Analysis of results shows the maximum of 1491X reduction in leakage power with the proposed method of balancing between sub-threshold leakage and BTBT leakage using leakage monitoring. Table 1 confirms the simulation results of each benchmark circuit at different temperatures of the circuit. Since the optimal body bias is also adjusted according to the temperature variations in the proposed approach, the results demonstrate that the leakage power is far less sensitive to the temperature variations.

CONCLUSION

This paper presents a novel leakage power minimizing technique in nanoscale CMOS integrated circuits by applying optimal reverse body bias to the substrate of transistors. The circuit detects the optimal body bias by monitoring the extracted sub-threshold leakage current ($I_{SUB}$) component and band-to-band tunneling leakage current ($I_{BTBT}$) component simultaneously. The simulation results demonstrate that the proposed optimal body biasing technique accomplishes a considerable energy reduction in nanoscale CMOS integrated circuits and the feedback loop of the proposed technique compensates for the temperature and supply voltage variations simultaneously.

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